

FlipKY®, 1 A



FlipKY®

FEATURES

- Ultralow V_F per footprint area
- Low thermal resistance
- One-fifth footprint of SMA
- Super low profile (< 0.7 mm)
- Available tested on tape and reel
- Small footprint, surface mountable
- Low forward voltage drop
- High frequency operation
- Guard ring for enhanced ruggedness and long term reliability
- Designed for consumer level

DESCRIPTION

True chip-scale packaging is available from Vishay HPP. The FCSP130ETR surface mount Schottky rectifier has been designed for applications requiring low forward drop and very small footprints on PC boards. Typical applications are in disk drives, switching power supplies, converters, freewheeling diodes, battery charging, and reverse battery protection.

The FlipKY® package, is one-fifth the footprint of a comparable SMA package and has a profile of less than 0.7 mm. Combined with the low thermal resistance of the die level device, this makes the FlipKY the best device for applications where printed circuit board space is at a premium and in extremely thin application environments such as battery packs, cell phones and PCMCIA cards.

PRODUCT SUMMARY

$I_{F(AV)}$	1 A
V_R	30 V

MAJOR RATINGS AND CHARACTERISTICS

SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_{F(AV)}$	Rectangular waveform	1.0	A
V_{RRM}		30	V
I_{FSM}	$t_p = 5 \mu s$ sine	220	A
V_F	1.0 Apk, $T_J = 125^\circ C$	0.33	V
T_J	Range	- 55 to 150	$^\circ C$

VOLTAGE RATINGS

PARAMETER	SYMBOL	FCSP130ETR	UNITS
Maximum DC reverse voltage	V_R	30	V
Maximum working peak reverse voltage	V_{RWM}		



ABSOLUTE MAXIMUM RATINGS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average forward current	I _{F(AV)}	50 % duty cycle at T _{PCB} = 120 °C, rectangular waveform		1.0	A
Maximum peak one cycle non-repetitive surge current at 25 °C	I _{FSM}	5 μs sine or 3 μs rect. pulse	Following any rated load condition and with rated V _{RRM} applied	220	
		10 ms sine or 6 ms rect. pulse		21	
Non-repetitive avalanche energy	E _{AS}	T _J = 25 °C, I _{AS} = 2.0 A, L = 5.0 mH		10	mJ
Repetitive avalanche current	I _{AR}	Current decaying linearly to zero in 1 μs Frequency limited by T _J maximum V _A = 1.5 x V _R typical		2.0	A

ELECTRICAL SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS		TYP.	MAX.	UNITS
Maximum forward voltage drop	$V_{FM}^{(1)}$	1 A	$T_J = 25\text{ }^{\circ}\text{C}$	0.41	0.45	V
		2 A		0.46	0.50	
		1 A	$T_J = 125\text{ }^{\circ}\text{C}$	0.29	0.33	
		2 A		0.37	0.40	
Maximum reverse leakage current	$I_{RM}^{(1)}$	$V_R = \text{Rated } V_R$	$T_J = 25\text{ }^{\circ}\text{C}$	30	100	μA
			$T_J = 125\text{ }^{\circ}\text{C}$	10	30	mA
Maximum junction capacitance	C_T	$V_R = 5\text{ V}_{DC}$ (test signal range 100 kHz to 1 MHz) $25\text{ }^{\circ}\text{C}$		-	210	pF
Maximum voltage rate of charge	dV/dt	Rated V_R		-	10 000	V/ μs

Note

(1) Pulse width < 300 μs , duty cycle < 2 %

THERMAL - MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction and storage temperature range	$T_J^{(1)}, T_{Stg}$		- 55 to 150	$^{\circ}\text{C}$
Typical thermal resistance, junction to PCB	$R_{thJL}^{(2)}$	DC operation	40	$^{\circ}\text{C/W}$
Maximum thermal resistance, junction to ambient	R_{thJA}		62	

Notes

(1) $\frac{dP_{tot}}{dT_J} < \frac{1}{R_{thJA}}$ thermal runaway condition for a diode on its own heatsink

(2) Mounted on 1" square PCB

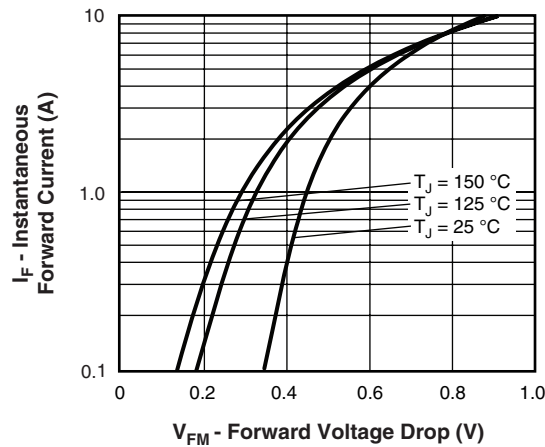


Fig. 1 - Maximum Forward Voltage Drop Characteristics (Per Leg)

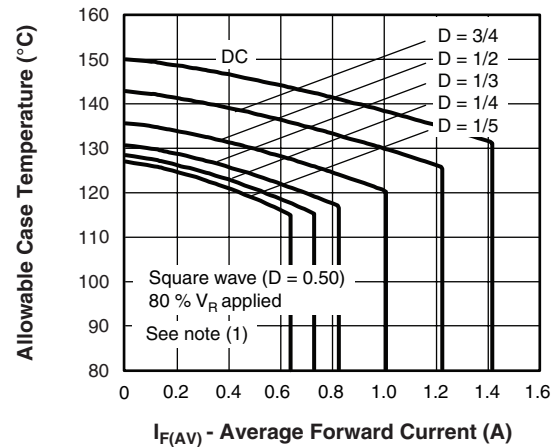


Fig. 4 - Maximum Allowable Case Temperature vs. Average Forward Current (Per Leg)

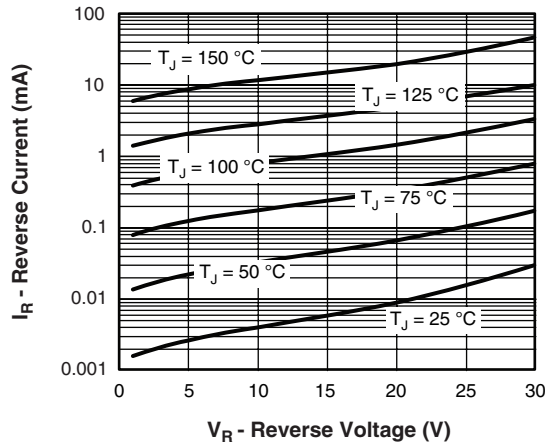


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage (Per Leg)

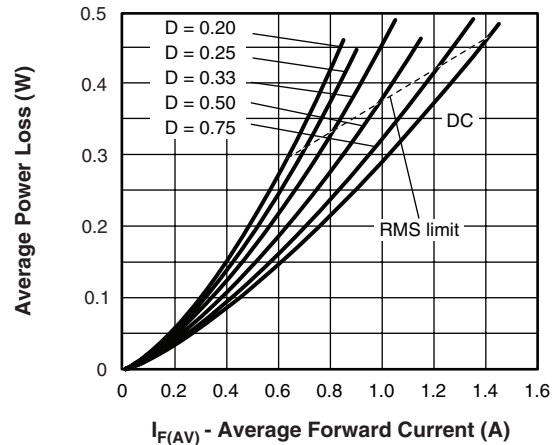


Fig. 5 - Forward Power Loss Characteristics (Per Leg)

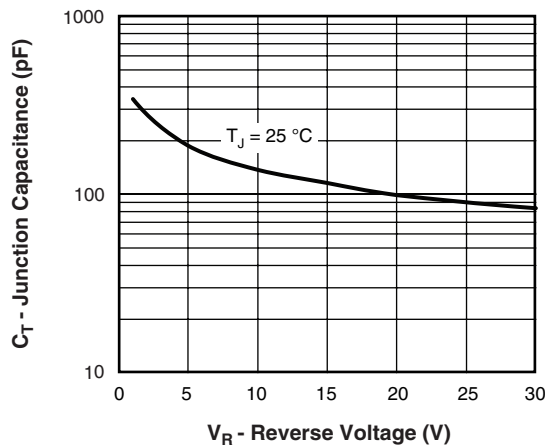


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage (Per Leg)

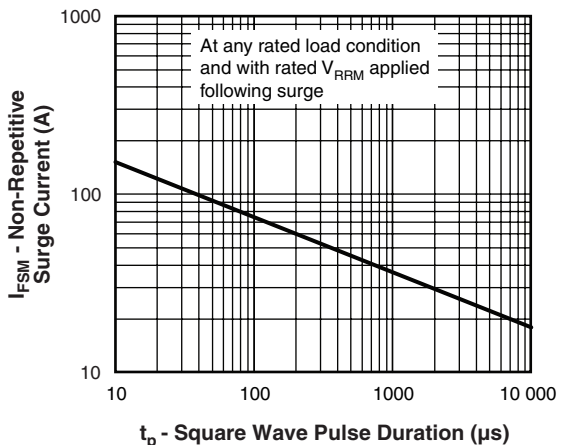


Fig. 6 - Maximum Non-Repetitive Surge Current (Per Leg)

Note

(1) Formula used: $T_C = T_J - (P_d + P_{dREV}) \times R_{thJC}$

P_d = Forward power loss = $I_{F(AV)} \times V_{FM}$ at $(I_{F(AV)}/D)$ (see fig. 6); P_{dREV} = Inverse power loss = $V_{R1} \times I_R (1 - D)$; I_R at 80 % V_R applied

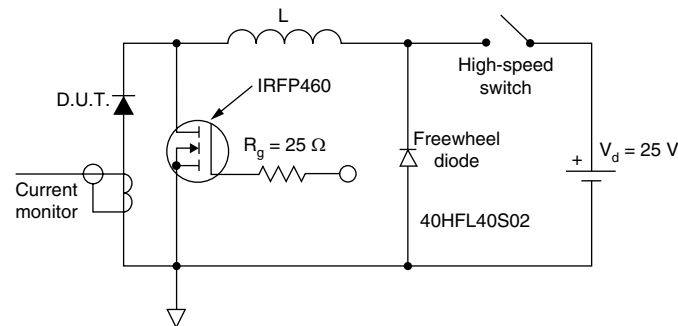


Fig. 7 - Unclamped Inductive Test Circuit

LINKS TO RELATED DOCUMENTS	
Dimensions	http://www.vishay.com/doc?95359
Part marking information	http://www.vishay.com/doc?95281
Packaging information	http://www.vishay.com/doc?95062



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