PSMN2R6-80YSF

NextPower 80 V, 2.7 mOhm, 218 A, N-channel MOSFET in LFPAK56E package

27 April 2023 — Objective data sheet

1. General description

NextPower 80 V, standard level gate drive MOSFET. Qualified to 175 °C and recommended for industrial and consumer applications.

2. Features and benefits

- Low Q_{rr} for higher efficiency and lower spiking
- 218 A $I_{D(max)}$ – demonstrated continuous current rating
- Low $Q_G \times R_{DSon}$ FOM for high efficiency switching applications
- Strong avalanche energy rating (E_{as})
- Avalanche rated and 100% tested
- Ha-free and RoHS compliant LFPAK56E package

3. Applications

- Synchronous rectifier in AC-DC and DC-DC
- Primary side switch in DC-DC
- BLDC motor control
- USB-PD adapters
- Full-bridge and half-bridge applications
- Flyback and resonant topologies

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	80	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C		-	-	218	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	294	W
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C		-	2.3	2.7	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 100 °C		-	3.6	4.3	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 40 V; V_{GS} = 10 V		[tbd]	15	[tbd]	nC
$Q_{G(tot)}$	total gate charge			[tbd]	83	[tbd]	nC
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 58 A; V_{sup} ≤ 80 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; t_p = 127 µs; Fig. 2	[1]	-	-	382	mJ

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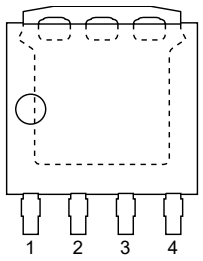
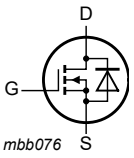
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Source-drain diode							
Q_r	recovered charge	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 40 V; Fig. 6		-	27	-	nC

[1] Protected by 100% test

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 **LFPAK56E; Power-SO8 (SOT1023)**	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN2R6-80YSF	LFPAK56E; Power-SO8	plastic, single-ended surface-mounted package (LFPAK56); 4 leads; 1.27 mm pitch	SOT1023

7. Limiting values

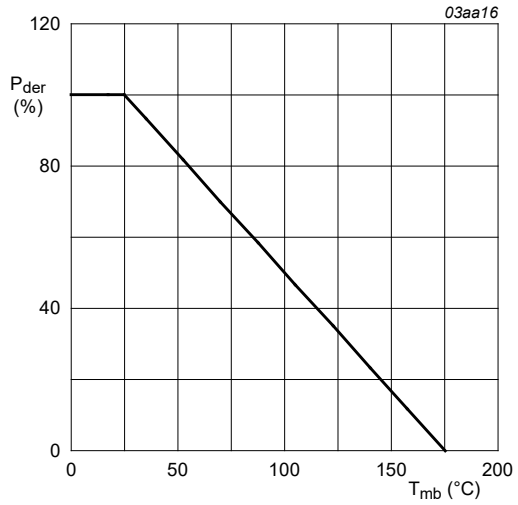
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). T_j =25 °C, unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	80	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ		-	80	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	294	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C		-	218	A
		V_{GS} = 10 V; T_{mb} = 100 °C		-	154	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	871	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	218	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	871	A

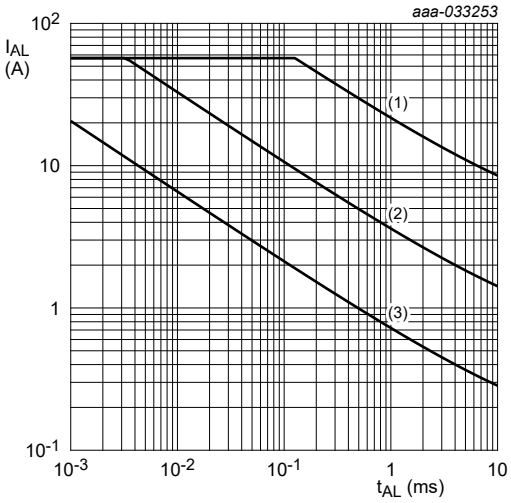
Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 58 A; $V_{sup} \leq$ 80 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; t_p = 127 µs; Fig. 2	[1]	-	382	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq$ 80 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω; Fig. 2	[1]	-	58	A

[1] Protected by 100% test



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



(1) $T_{j(init)}$ = 25 °C; (2) $T_{j(init)}$ = 150 °C; (3) Repetitive Avalanche

Fig. 2. Avalanche rating; avalanche current as a function of avalanche time

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 3		-	0.45	0.51	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 4		-	42	-	K/W
		Fig. 5		-	85	-	K/W

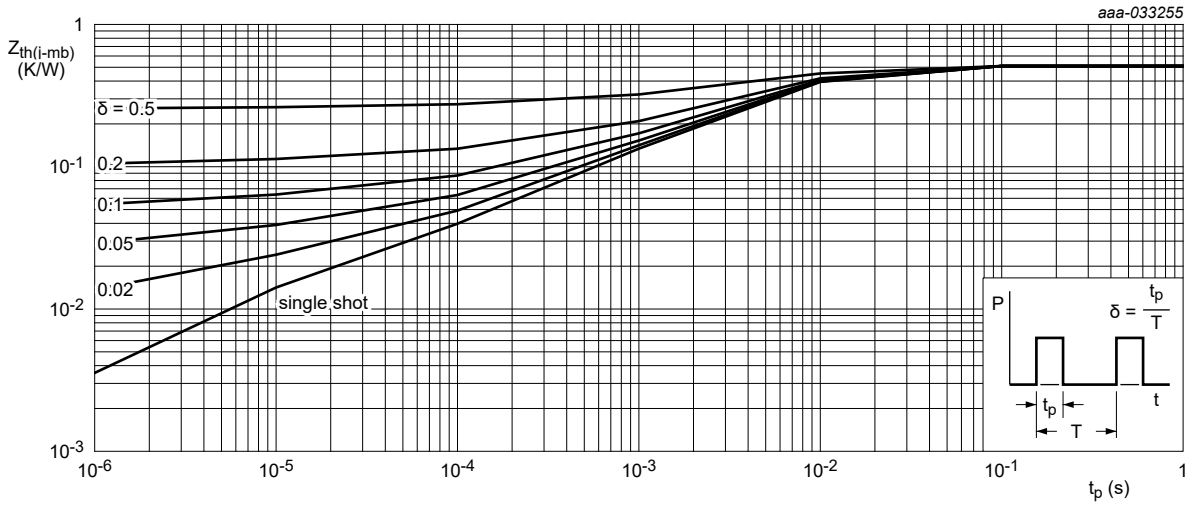
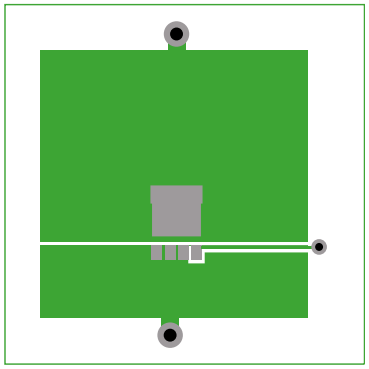
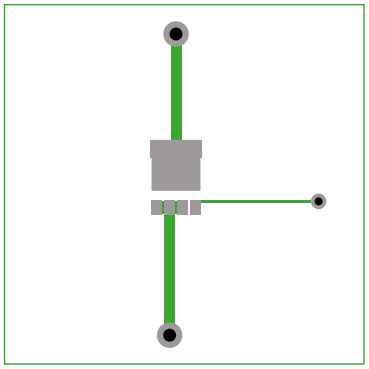


Fig. 3. Transient thermal impedance from junction to mounting base as a function of pulse duration



Copper area 25.4 mm square; 70 µm thick on FR4 board

Fig. 4. PCB layout for thermal resistance from junction to ambient



70 µm thick copper on FR4 board

Fig. 5. PCB layout with minimum footprint for thermal resistance from junction to ambient

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		80	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		72	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C		2.2	3	3.8	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C		-	1.8	-	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C		-	3.4	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	25 °C ≤ T_j ≤ 150 °C		-	-7.2	-	mV/K
I_{DSS}	drain leakage current	V_{DS} = 80 V; V_{GS} = 0 V; T_j = 25 °C		-	0.07	1	µA
		V_{DS} = 80 V; V_{GS} = 0 V; T_j = 125 °C		-	2	100	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C		-	2.3	2.7	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 100 °C		-	3.6	4.3	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C		-	5.1	6.1	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		[tbd]	0.7	[tbd]	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 40 V; V_{GS} = 10 V		[tbd]	83	[tbd]	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V		-	43	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 40 V; V_{GS} = 10 V		[tbd]	25.2	[tbd]	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	16.5	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	8.7	-	nC
Q_{GD}	gate-drain charge			[tbd]	15	[tbd]	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 40 V		-	4.5	-	V
C_{iss}	input capacitance	V_{DS} = 40 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C		[tbd]	6150	[tbd]	pF
C_{oss}	output capacitance			[tbd]	1736	[tbd]	pF
C_{rss}	reverse transfer capacitance			[tbd]	41	[tbd]	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 40 V; R_L = 1.6 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω		-	22	-	ns
t_r	rise time			-	17	-	ns
$t_{d(off)}$	turn-off delay time			-	46	-	ns
t_f	fall time			-	24	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C		-	0.8	1	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 40 V; Fig. 6		-	33	-	ns
Q_r	recovered charge			-	27	-	nC

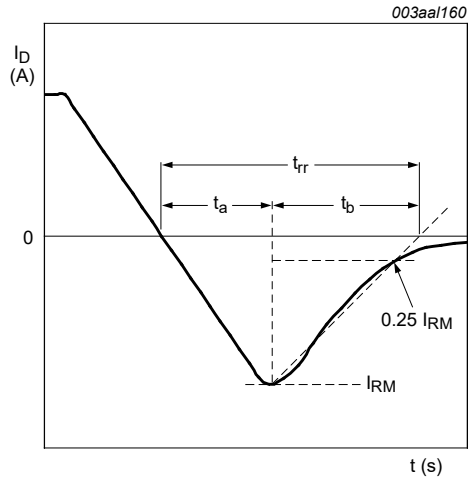
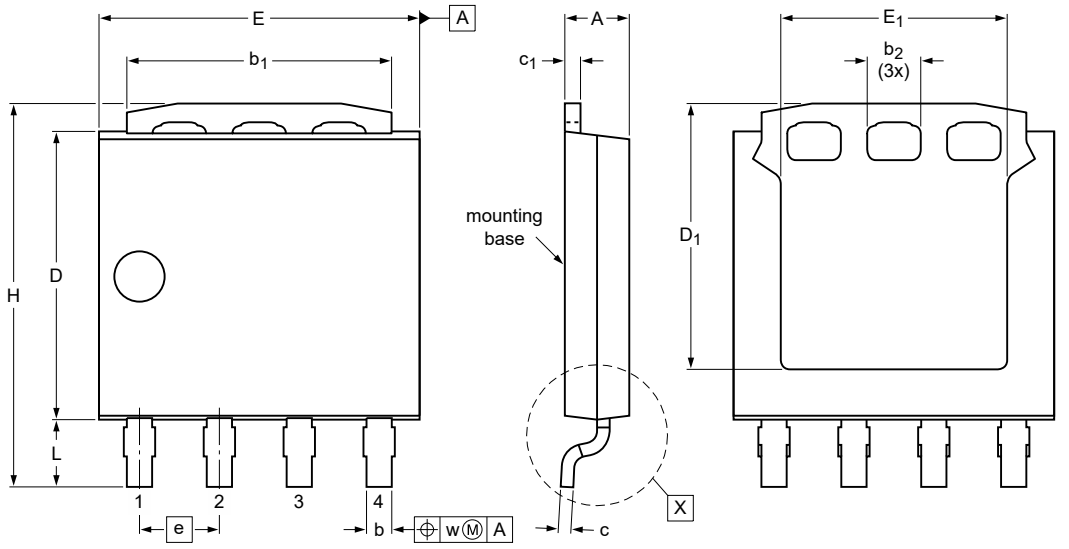


Fig. 6. Reverse recovery timing definition

10. Package outline

Plastic single-ended surface-mounted package (LFPAK56E); 4 leads **SOT1023**



0 2.5 5 mm

scale

Dimensions

Unit		A	A_1	b	b_1	b_2	c	c_1	$D^{(1)}$	$D_1{}^{(1)}$	$E^{(1)}$	$E_1{}^{(1)}$	e	H	L	L_p	w	y	θ
mm	max	1.10	0.15	0.50	4.41		0.25	0.30	4.70	4.45	5.30	3.7		6.2	1.3	0.85			8°
	nom					0.85							1.27				0.25	0.1	
	min	0.95	0.00	0.35	3.62		0.19	0.24	4.45		4.95	3.5		5.9	0.8	0.40			0°

Note

1. Plastic or metal protrusions of 0.15 mm per side are not included.

sot1023_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1023						~~13-03-05~~ 17-07-31

Fig. 7. Package outline LFPAK56E; Power-SO8 (SOT1023)

11. Soldering

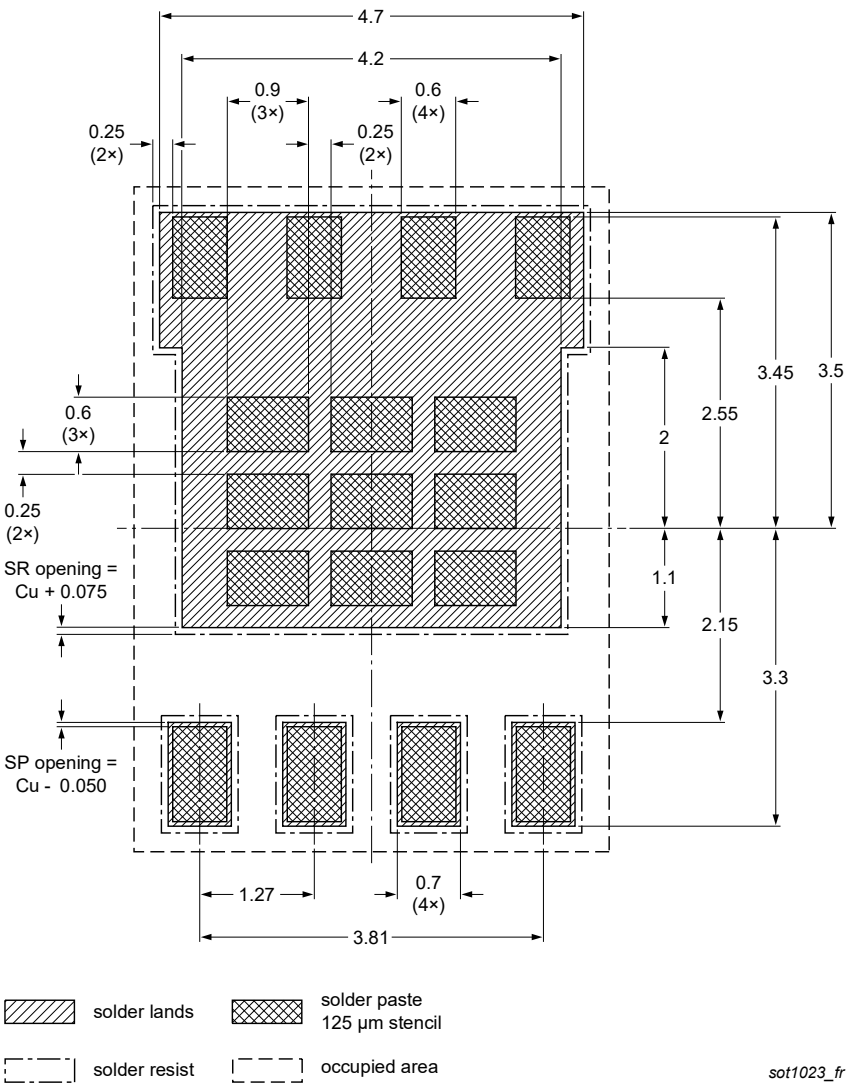


Fig. 8. Reflow soldering footprint for LFPAK56E; Power-SO8 (SOT1023)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".
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